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09/385,394	08/30/1999	JOHN S. YATES JR.	AMD-004000	9093

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
11/24/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eoffice@volpe-koenig.com

Office Action Summary	Application No.	Applicant(s)	
	09/385,394	YATES ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-36,60,63,69,71-73,75 and 86* is/are allowed.

6)☒ Claim(s) *1-7,9-12,14-19,21,37-47,49,50,113-116,119,121-126 and 128-133* is/are rejected.

7)☒ Claim(s) *20,48 and 127* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/25/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-7,9-12,14-21,34-50,60,63,69,71-73,75,86,113-116,119 and 121-133.

1. Claims 1-7, 9-12, 14-21, 34-50, 60, 63, 69, 71-73, 75, 86, 113-116, 119 and 121-133 are presented for examination.

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR § 1.67(a) identifying this application by Serial Number and filing date is required. See MPEP § 602.01 and § 602.02.

The oath or declaration is defective because:

A. Non-initialed and/or non-dated alterations have been made to the oath or declaration See 37 CFR § 1.52(c).

In both of the November 12, 1999 and December 13, 1999 filings, the address of inventor "T R Ramesh" has been altered, but the alterations themselves have not been initialed and dated by the inventor.

In both of the November 12, 1999 and December 13, 1999 filings, the name of inventor "John S. Yates" has been altered to add ", Jr.", but the alteration itself has not been initialed and dated by the inventor.

B. The full name of each inventor (family name and at least one given name together with any initial) has not been set forth. See 37 CFR § 1.63(a)(2).

In all three declarations filed August 30, 1999, November 12, 1999 and December 13, 1999 the name of inventor "T R Ramesh" is listed without providing at least one given name to accompany the family name.

3. The computer program listing filed on August 30, 1999 as a "microfiche appendix" is unacceptable. A computer program listing conforming to the requirements of 37 CFR § 1.96 is required.

The microfiche appendix is unacceptable because it is not limited to containing only a computer program listing. There appear to be at least six tables, and two graphical flowcharts contained within the frames of the appendix. Both of which are not a computer program listing as defined by MPEP 608.05(a). Applicant is reminded that in resubmitting the appendix in proper format, he must adhere to the new 37 CFR 1.96 rules regarding submission of a

computer program listing because as of February 28, 2001, the office no longer accepts microfiche.

4. The attempt to incorporate subject matter into this application by reference to US Patent applications 09/322,443, 09/298,536, and 09/239,194 is improper because those applications themselves incorporate by reference additional subject matter. See MPEP 608.01(p)(A).

5. The attempt to incorporate subject matter into this application by reference to a list of publications on pg. 143 is improper because applicant may not incorporate essential material by reference to a document which is not a US patent or US patent publication.

6. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

8. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

9. The indicated allowability of claims 1-7, 9-12, 14-19, 21, 37-47, 49-50, 113-116, 119, 121-126 and 128-133 is withdrawn in view of the newly discovered prior art to Mourey et al.,

US Patent 5,452,456. Rejections based on the newly discovered prior art follow.

10. Claims 4, 9-10, 14-18, 21, 37, 40-45, 47, 49-50, 113-116, 119, 121, 123-126 and 133 are rejected under 35 USC § 102(b) as being anticipated by Mourey et al., U.S. Patent 5,452,456. Grohoski, *Machine organization of the IBM RISC System/6000 processor*, January 1990, is incorporated by reference into the specification of Mourey et al. at col. 1 line 62 to col. 2 line 2).

Mourey et al. taught (e.g. see figs. 1-7) the invention as claimed (as per claim 4), including a data processing ("DP") system comprising:

A. a method, comprising;

B. executing instructions (fig. 1, "CODE SEG.") fetched from first and second regions (18a, 18b, 18c) of a memory (16) of a computer (10), the instructions of the first and second regions being coded for execution by computers of first and second architectures or following first and second data storage conventions (col. 3 lines 26-35, col. 4 lines 7-17), respectively, the memory regions having associated first and second indicator elements (20, fig. 2, 31), the indicator elements each having a value indicating the architecture or data storage convention under which instructions from the associated region are to be executed (col. 3 lines 26-35, col. 5 lines 5-58), the first architecture having a pre-defined, established definition (col. 1 line 58 to col. 2 line 14), the computer providing an implementation of the first architecture (col. 3 lines 18-26);

C. when execution of the instruction data flows or transfers from the first region to the second region (col. 8 lines 36-50), adapting the computer for execution in the second architecture or data storage convention (col. 8 lines 63-68, col. 9 line 60 to col. 10 line 49, fig. 6a1, 6a2).

11. As to claim 9, Grohoski (incorporated by reference into Mourey et al. at col. 1 line 62 to col. 2 line 2) taught on pg. 39 that the IBM RISC System/6000 processor possessed an instruction cache (fig. 1). Accordingly, the executable regions will be lines in the instruction

cache when the regions are resident in the instruction cache.

12. As to claim 10, Mourey et al. taught that the two architectures were two instruction set architectures (col. 1 line 58 to col. 2 line 2); and

the adapting includes controlling instruction execution hardware of the computer to interpret the instructions according to the two instruction set architectures according to the indicator elements (col. 3 lines 18-26, col. 2 lines 58-60, col. 4 lines 7-13).

13. As to claim 14, Mourey et al. taught that a mode of execution of the instructions was changed without software intervention when execution flowed or transferred from the first region to the second region (col. 4 lines 12).

14. As to claim 15, Mourey et al. taught that execution of the computer took an exception when execution flowed or transferred from the first region to the second region (col. 3 lines 36-39).

15. As to claim 16, Mourey et al. taught that the mode of execution of the instructions was explicitly controlled by an exception handler (col. 3 lines 36-39, col. 3 lines 56-59).

16. As to claims 17 and 41, Mourey et al. taught one of the regions stored an operating system binary coded in an instruction set non-native to the computer (col. 4 lines 18-27), the non-native instruction set providing access to a reduced subset of the resources of the computer (col. 4 lines 7-18).

17. As to claim 18, Mourey et al. taught recognizing when program execution has flowed or transferred from a region whose indicator element indicates the first data storage convention to a region whose indicator element indicates the second data storage convention, and in response to the recognition, altering the data storage content of the computer to create a program context under the second data storage convention that is logically equivalent to a pre-alteration program context under the first data storage convention (fig. 6a1, 6a2).

18. As to claim 21, Mourey et al. taught that the instruction data coded for execution a a first of the two instruction set architectures observed a first data storage convention associated with the first architecture (col. 10 lines 18-19), and instruction data coded for execution by a

second of the two instruction set architectures observed a second data storage convention associated with the second architecture (fig. 6a1, "MOVE PARAMETERS DEFINED IN PROCEDURE INFORMATION FIELD FROM THE 68K STACK INTO RISC REGISTERS"), the second data storage convention being different from the first data storage convention (fig. 6a1, stack convention to register convention), a single indicator element indicating both the instruction set architecture and the data storage convention (fig. 2, 20), and further comprising recognizing when program execution flowed for transferred from a region using the first instruction set architecture to a region using the second instruction set architecture, and in response to the recognition, adjusting the data storage content of the computer from the first data storage convention to the second data storage convention (fig. 6a1, 6a2).

19. As to claims 37, 43, 45, and 50, they do not teach or define above the invention claimed in claims 4, 9-10, 14-18 and 21 and are therefore rejected under Mourey et al. for the same reasons set fourth in the rejection of claims 4, 9-10, 14-18 and 21, supra.

20. As to claim 40, Mourey et al. taught that the two architectures were two instruction set architectures (col. 1 line 58 to col. 2 line 2), and
further comprising processor pipeline control circuitry designed to control the pipeline to effect interpretation of the instructions under the two instruction set architectures alternately, according to the associated indicator elements (col. 3 lines 19-26).

21. As to claim 42, Mourey et al. taught that the indicator element was further designed to store an indication of a calling convention under which the instruction data of the associated region was coded for execution by the pipeline (col. 5 lines 54-58), and;
further comprising software programmed to alter the data storage content of a computer using the computer processor to create a program context under the second calling convention that is logically equivalent to a pre-alteration program context under the first calling convention (figs. 6a1, 6a2);
the memory unit further designed to recognize when program execution has flowed or

transferred from a region whose indicator element indicates the first calling convention to a region whose indicator element indicates the second calling convention, and in response to the recognition, to invoke the transition management software (figs. 6a1, 6a2).

22. As to claim 44, Mourey et al. taught that the memory unit and software were designed to effect a transition between instruction boundaries, between execution in a region coded in the first instruction set using the first calling convention to execution in a region coded in the second instruction set using the second calling convention, so that code at the source of the flow or transfer may effect the execution transition without being specially coded for code at the destination (col. 4 lines 7-33).

23. As to claim 47, Mourey et al. taught that a rule for altering the data storage content from the first calling convention to the second calling convention was determined by examining a descriptor associated with the location of execution before the recognized execution flow or transfer (figs. 2, 6a1, 6a2).

24. As to claim 49, Mourey et al. taught a transition manager designed to effect a transition between the execution of code coded in instructions of a first instruction set architecture and code coded in instructions of a second instruction set architecture, the transition manger designed to alter a bit representation of a datum from a first representation under the first architecture to a second representation under the second architecture, the alteration of representation being chosen to preserve the meaning of the datum across the change in execution architecture (figs. 6a1, 6a2).

25. As to claims 113-116, 119, 121, 123, 126 and 133, they do not teach or define above the invention claimed in the above rejected claims and are therefore rejected under for the same reasons set fourth in the rejection of the above rejected claim, supra.

26. As to claims 124-125, Mourey et al. taught software or hardware designed to copy a datum from a first and third locations to a second and fourth locations, the first and third locations having a use under the first calling convention analogous to the use of the second and fourth locations under the second calling convention (figs. 6a1, 6a2).

As to claim 125, Mourey et al. taught that the software or hardware for the copying was programmed to assume that exactly one of the first and third locations was no longer required by the execution of the program (fig. 6a1, 6a2).

27. Claims 1-3, 5-7, 11-12, 19, 38-39, 46, 122 and 128-132 are rejected under 35 USC § 103 as being unpatentable over Mourey et al., U.S. Patent 5,452,456, in view of Goetz et al., U.S. Patent 5,854,913.

Goetz et al. was cited as a prior art reference in the last office action, mailed October 25, 2004.

28. As to claims 5, 11 and 19 Mourey et al. did not teach that the regions were pages managed by a virtual memory manager. Goetz et al. taught pages of a virtual memory manager containing information detailing an execution type or data storage convention of each page (col. 17 lines 34-49). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Goetz et al.'s suggestion of storing information detailing an execution type or data storage convention with each page of a virtual memory manager with Mourey et al.'s invention because of Goetz et al.'s teaching that doing so "allows for a more dynamic environment for running software written for both architectures in a multi-tasking operating system" and "allows a single operating system to manage address translation for software written for either architecture" (col 17 lines 50-64).

As to the additional feature of claim 19, Mourey et al. taught that one of the two data storage conventions was a register-based calling convention (figs. 6a1, 6a2, col. 11 lines 19-41), and the other data storage convention was a memory stack-based calling convention (figs. 6a1, 6a2, col. 11 lines 19-41).

29. As to claims 6 and 38, Mourey et al. taught that the indicator elements were stored in a table of indicator elements distinct from a primary address translation table used by the virtual memory manager (fig. 1, 20, fig. 2, 20), Goetz et al. taught associating the indicator elements of the table with corresponding pages of the memory (col. 17 lines 34-49).

30. As to claim 7, Mourey et al. taught that the indicator elements were stored in a table

(fig. 1, 20, fig. 2, 20), Goetz et al. taught associating each indicator element with a corresponding physical page frame (col. 17 lines 34-49).

31. As to claim 12, Mourey et al. taught that the indicator elements were stored in a table (fig. 1, 20, fig. 2, 20), Goetz et al. taught associating each indicator element with a corresponding physical page frame which would result in each entry being indexed by physical page frame number (col. 17 lines 34-49).

32. As to claims 1-3, they do not teach or define above the invention claimed in claims 4-7 9-12 and 14-21 and are therefore rejected under Mourey et al. in view of Goetz et al. for the same reasons set fourth in the rejection of claims 4-7 9-12 and 14-21, supra.

33. As to claim 39, Goetz et al. taught a translation look-aside buffer (TLB) (col. 17 lines 13-16) and TLB control circuitry designed to load the indicator elements into the TLB from a table stored in memory, the entries of the table being indexed by corresponding physical page frame number (both aspects are inherent given the presence of a TLB as detailed by Goetz et al.).

34. As to claims 46 and 122, Goetz et al. taught that the logical resources for support of first and second instruction set architectures were overlaid on physical resources of a computer processor according to a mapping that assigned corresponding resources of the two architectures to a common physical resource when the resource served analogous functions in the calling convention of the two architectures (col. 6 lines 16-25).

35. As to claims 128 and 130-131, they do not teach or define above the invention claimed in the above rejected claims and are therefore rejected under Mourey et al. in view of Goetz et al. for the same reasons set fourth in the rejection of the above rejected claims, supra.

36. As to claim 129, Goetz et al. taught storing the indicator elements in virtual address translation table entries (col. 17 lines 34-37).

37. As to claim 132, Goetz et al. taught that the indicator elements would have been stored in storage that is architecturally addressable when the pipeline is executing in one of the architectures and architecturally unaddressable when the pipeline was executing in the other

architecture (col. 17 lines 50-64).

38. Claims 20, 48 and 127 are objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

39. Claims 34-36, 60, 63, 69, 71-73, 75 and 86 are allowable over the prior art of record.

40. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

41. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

/Richard Ellis/
Primary Examiner, Art Unit 2183
November 12, 2010